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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,221	09/20/2006	Hajime Nagai	1176/309	5690
46852	7590	03/21/2008		
LIU & LIU 444 S. FLOWER STREET, SUITE 1750 LOS ANGELES, CA 90071				
EXAMINER				
TRAN, THIENVU V				
ART UNIT		PAPER NUMBER		
2819				
MAIL DATE		DELIVERY MODE		
03/21/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/566,221

Applicant(s)

NAGAI, HAJIME

Examiner

THIENVU V. TRAN

Art Unit

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Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-2, 9-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2 and 9-19 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☒ Claim(s) 20-24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 July 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF-08)
- Paper No(s)/Mail Date 1/26/2006, 1/18/2008.
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application.
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Aoki et al (U.S. Patent No. 5,192,879).

With respect to claim 1, Aoki teaches a converting device comprising:

a first input portion receiving a first input signal (e.g., input_1) (see fig. 4 below);
a first output portion outputting a first output signal (e.g., output_1) (see fig. 4 below);
a second input portion receiving a second input signal (e.g., input_2) (see fig. 4 below);
a second output portion outputting a second output signal (e.g., output_2) (see fig. 4 below); and
a voltage dropping circuit (e.g., circuit containing transistors 2N, 2P, 1N, 1P) (see fig. 4) dropping voltages on a first node (e.g., node_1) (see fig. 4 below) located between said first input portion and said first output portion to ground voltage (e.g., when a low signal appears at the gate of transistors 2N and 2P, transistor 2P will turn on and 2N will turn off, thereby placing the node *node_1* at ground) (see fig. 4 below) and on a second node (e.g., node_2) (see fig. 4 below) located between said second input portion and said second output portion to ground voltage (e.g., when a high signal appears at the gate of transistors 1N and 1P, transistor 1N will turn on and 1P will turn off, thereby

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placing the node *node_2* at ground) (see fig. 4 below), before changing from a state in which said first input portion is disconnected from said first node to a state in which said first input portion is connected to said first node (e.g., the node *node_1* is connected to the first input portion based on the control signal asserting and de-asserting transistor 2N/2P) (see fig. 4 below).

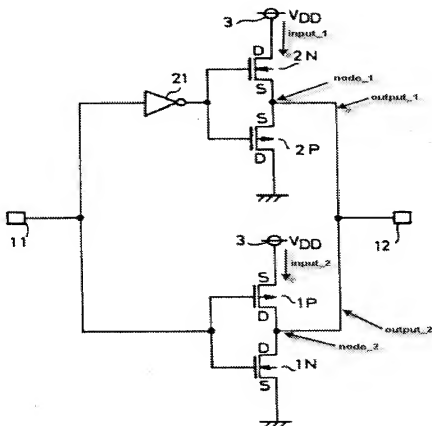


FIG. 4

Allowable Subject Matter

3. Claims 2, 9-19 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 2, the prior art does not fairly teach or suggest the claimed limitation as a whole, such a voltage converting device for receiving a first input signal having a first high input voltage and a first low input voltage and a second input signal having a second high input voltage and a second low input voltage, said first high input voltage having a relatively high voltage level and said first low input voltage having a relatively low voltage level, and said second high input voltage having a relatively high voltage level and said second low input voltage having a relatively low voltage level, wherein said voltage converting device converts at least one of said first high input voltage and said first low input voltage and outputs said first input signal having a converted voltage level as a first output signal and conveys at least one of said second high input voltage and said second low input voltage and outputs said second input signal having a converted voltage level as a second output signal, wherein said voltage converting device comprises: a first input portion receiving said first input signal; a first output portion outputting said first output signal; a second input portion receiving said second input signal; a second output portion outputting said second output signal; and a voltage converting circuit converting at least one of said first high input voltage and said first low input voltage and at least one of said second high input voltage and said second low input voltage, and wherein said voltage converting circuit comprises a first voltage dropping circuit dropping a voltage on a first node located between said first input portion and said first output portion to ground voltage before changing from a state in which said first input portion is disconnected from said first node to a state in which said first input portion is connected to said first node; and a second voltage dropping

circuit dropping a voltage on a second node located between said second input portion and said second output portion to ground voltage before changing from a state in which said second input portion is disconnected from said second node to a state in which said second input portion is connected to said second node.

With respect to claims 9-19, they depend on claim 2 above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. **Claims 20-24** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIENVU V. TRAN whose telephone number is (571)270-1276. The examiner can normally be reached on Monday-Friday (7:30AM-5:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T.T/

/Rexford N BARNIE/

Supervisory Patent Examiner, Art Unit 2819